

REALTEK

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**RTL8752CJ, RTL8752CJF
RTL8752CRF, RTL8752CGF**

BLUETOOTH LOW ENERGY SOC

PRELIMINARY DATASHEET
(CONFIDENTIAL: Development Partners Only)

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This document is intended for the software engineer’s reference and provides detailed programming information.

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REVISION HISTORY

Revision	Release Date	Summary
0.7	2018/06/20	Preliminary release.
0.71	2018/06/28	Corrected Table 30 Ordering Information, page 44.
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0.91	2018/11/28	Corrected minor typing errors.

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1. General Description

1.1. Overview

The RTL8752CJ/ RTL8752CJF/ RTL8752CRF/ RTL8752CGF (hereafter referred to as the RTL8752C except where differences exist) is an ultra-low-power system on-chip solution for Bluetooth 4.2 low energy applications that combines the excellent performance of a leading RF transceiver with a low-power ARM Cortex-M4F and rich powerful supporting features and peripherals.

The RTL8752C supports an analog MIC interface that integrates a sigma-delta ADC, programmable gain amplifier, 5-Band equalizer and microphone bias circuit for voice command application. The RTL8752C embeds IR transceiver, hardware key-scan, and Quad-decoder on a single IC, and is provided in a QFN package.

1.2. MCU Platform

The embedded ARM Cortex-M4F 32-bit CPU features a 16-bit instruction set with 32-bit extensions (Thumb-2® technology) that delivers high-density code with a small memory footprint. By using a single-cycle 32-bit multiplier, a 3-stage pipeline, and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex-M4F makes program execution simple and highly efficient.

Serial Wire Debug (SWD) interface provided as part of the Debug Access Port (DAP), in conjunction with the Basic Branch Buffer (BBB). This offers a flexible and powerful mechanism for non-intrusive program code debugging. Developers can easily add breakpoints in the code and perform single-step debugging.

The RTL8752C memory architecture includes ROM, 160kByte RAM and 8MByte Flash Address Space.

The 160kByte RAM consists of RAM1 (112kByte Data RAM), RAM2 (8kByte Cache Shared RAM), RAM3 (8kByte Cache Shared RAM), and RAM4 (32kByte Buffer RAM). All the RAM regions can be used to execute code and hold data.

Flash Address Space is a virtual space which is mapped to external Flash to extend the code space in XIP (eXecute In Place) mode.

1.3. RTL8752C Memory Architecture

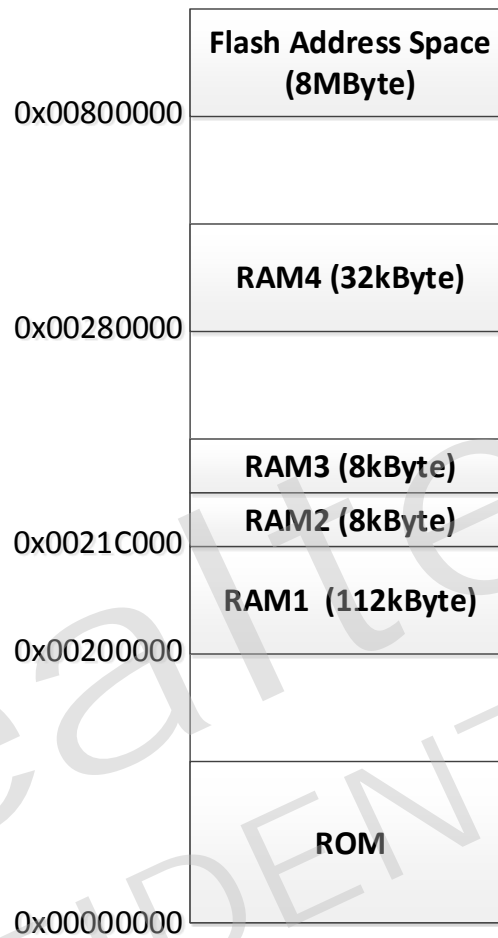


Figure 1. RTL8752C Memory Architecture

2. Features

General

- Ultra low power consumption with intelligent PMU
- Supports Bluetooth 4.2 core specification
- Additional Adv channel
- Channel Selection #2
- High Duty Cycle Non-Connectable Adv
- Integrated MCU to execute Bluetooth protocol stack
- Supports multiple level Low Energy states
- Supports LE L2CAP Connection Oriented Channel Support
- Supports LE low duty directed advertising
- Supports LE data length extension feature
- Supports OTA (Over-the-Air) programming mechanism for firmware upgrade
- Supports GAP, ATT/GATT, SMP, L2CAP
- Generic Applications for GAP Central, Peripheral, Observer and Broadcaster Roles

Platform

- ARM Cortex-M4 with floating-point unit (Maximum 20MHz)
- Serial flash controller (One Dual and Quad-bits mode) with 16kB 4-way cache. (Quad-bit mode is only in RTL8752CJ/CK)
- Total 160kB SRAM
- 4Kbits eFUSE for manufacturer use
- Supports AES128/192/256 encrypt/decrypt engine
- Embedded 2Mbits flash (RTL8752CJF/CRF/CGF)

Bluetooth Transceiver

- RX sensitivity: -97dBm BLE (min)
- TX output power: +4dBm (max)
- Fast AGC control to improve receiving dynamic range
- Supports Bluetooth Low Energy PHY

Peripheral Interfaces

- Flexible General Purpose IOs
RTL8752CJ: 24GPIOs (max)
RTL8752CJF: 26GPIOs (max)
RTL8752CRF: 18GPIOs (max)
RTL8752CGF: 18GPIOs (max)
- Hardware Keyscan and Quad-decoder
- Embedded IR transceiver
- Real-Time Counters (RTC)
- Supports generic 4-wire SPI master/slave (max clock rate: 10MHz)
- Supports 8 channel Low power comparator
- 400ksps, 12bit, 8-channel AUXADC
- Timers x 8
- I2C x 2
- PWM x 8
- UART x 2
- Supports external 40MHz XTAL without capacitor (in limited condition)
- Supports external 32.768kHz XTAL without capacitor (in limited condition)
- Supports embedded internal 32K RCOSC to keep BLE link (in limited condition)

- Embedded PGA and audio ADC with 5-band EQ for analog MIC interface (not available in RTL8752CGF)

Package

- RTL8752CJ: 40-pin 5x5mm QFN
- RTL8752CJF: 40-pin 5x5mm QFN
- RTL8752CRF: 32-pin 5x5mm QFN
- RTL8752CGF: 32-pin 5x5mm QFN

3. Applications

- TV Remote Controller
- LE HID
- Beacon
- Home Automation
- Key Fob
- Wristband
- Wearable Device
- Toy

4. Block Diagrams

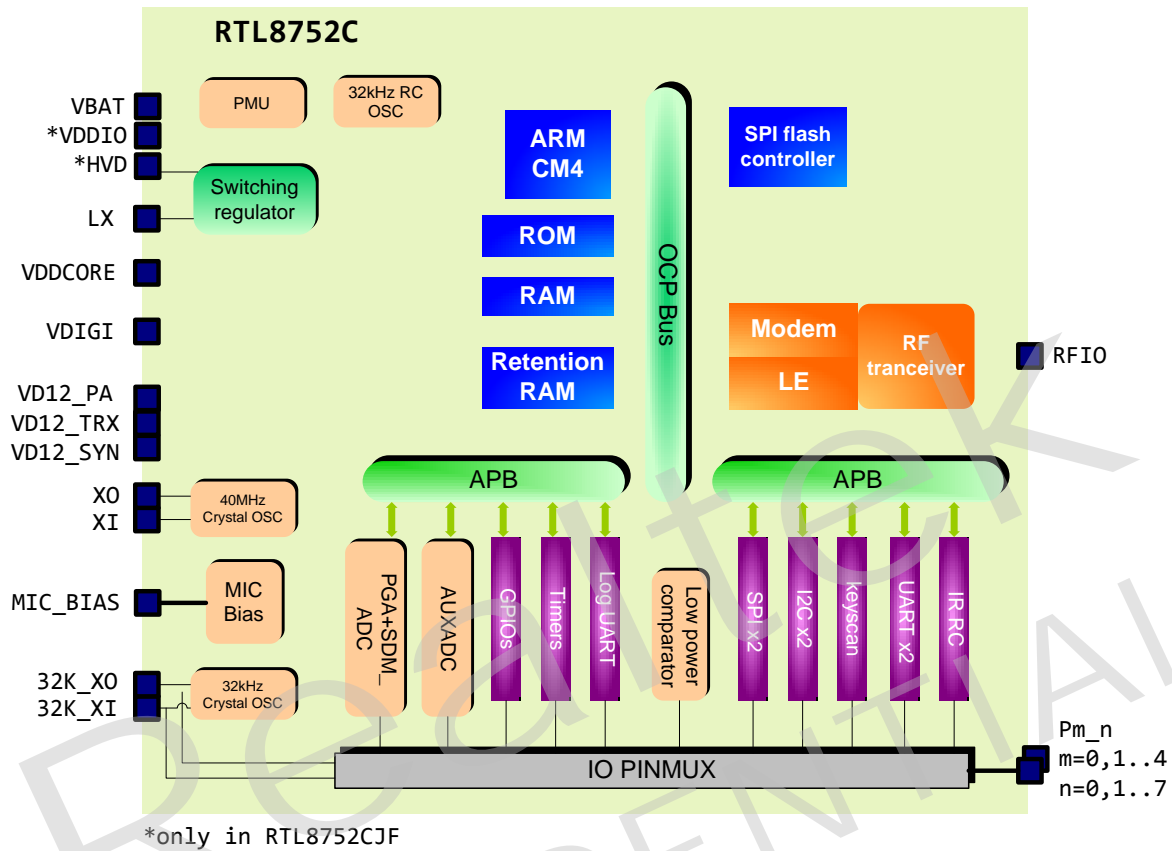


Figure 2. Block Diagram

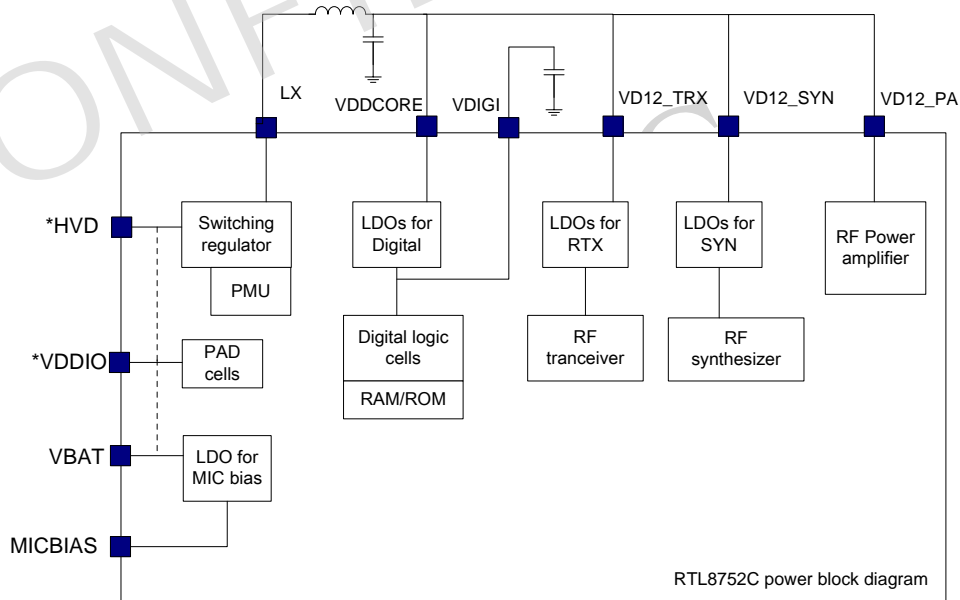


Figure 3. Power Block Diagram

5. Pin Assignments

5.1. RTL8752CJ Pin Assignments

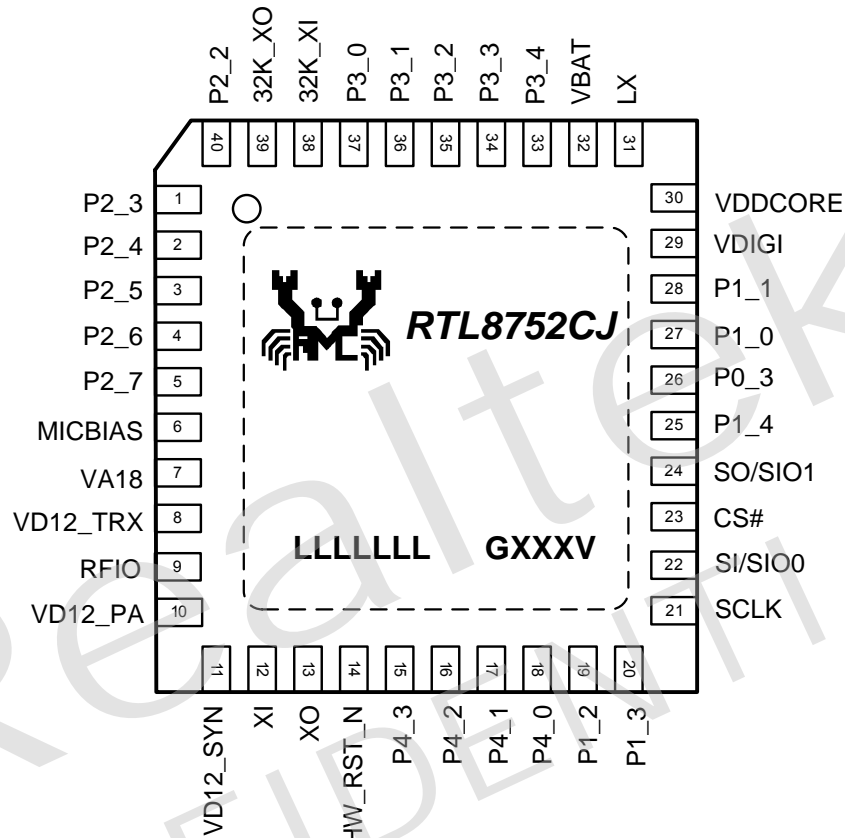


Figure 4. RTL8752CJ Pin Assignments

5.2. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 4).

5.3. RTL8752CJF Pin Assignments

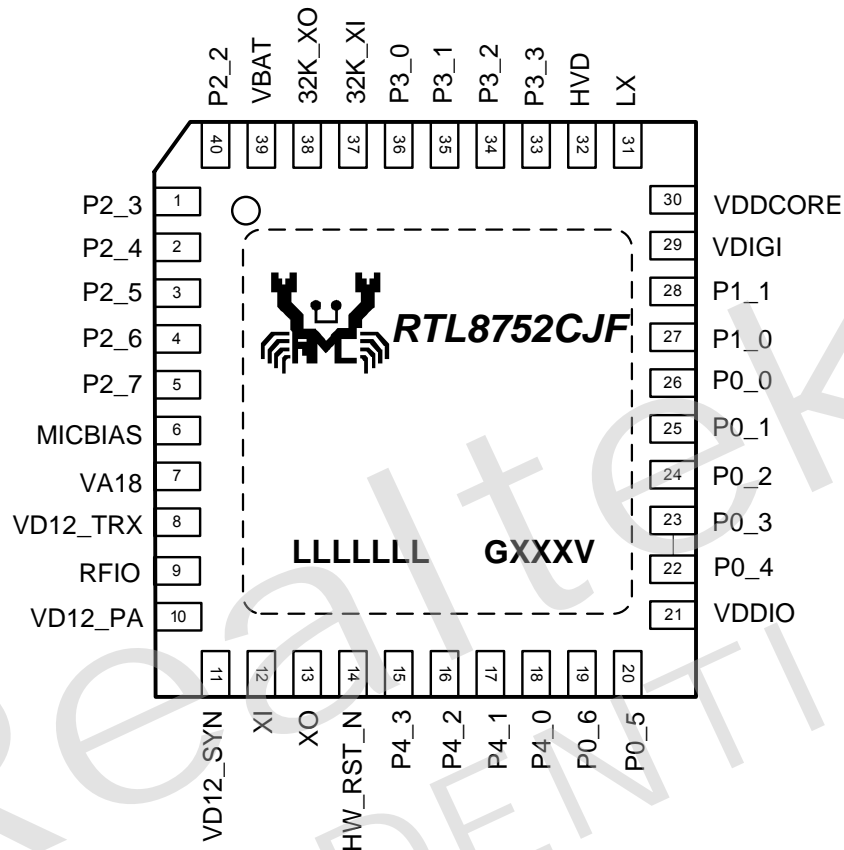


Figure 5. RTL8752CJF Pin Assignments

5.4. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 5).

5.5. RTL8752CRF Pin Assignments

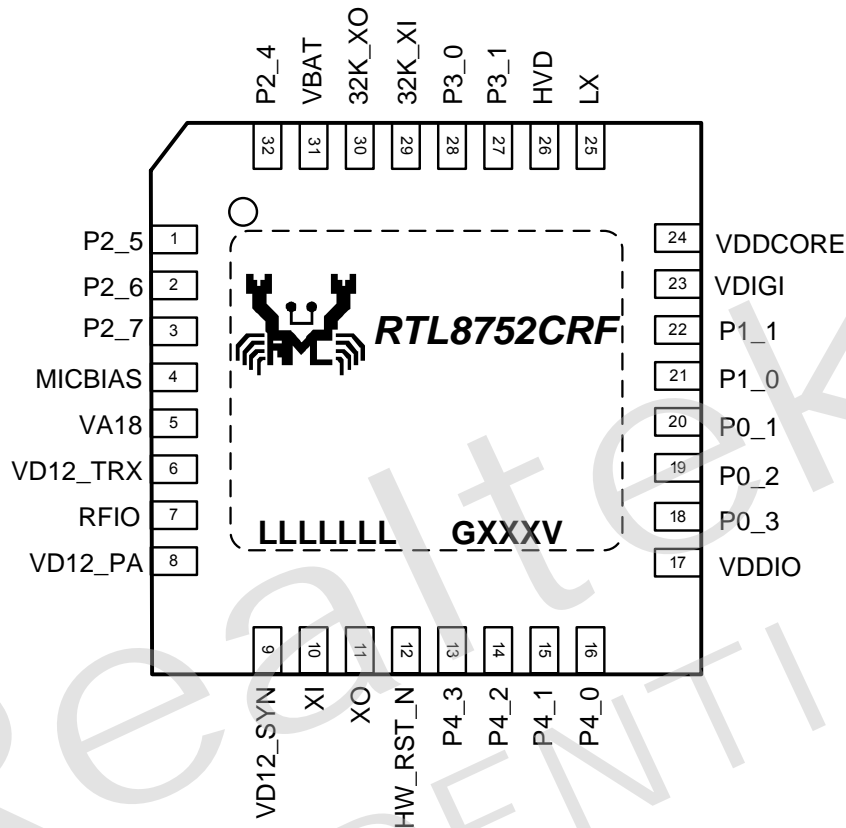


Figure 6. RTL8752CRF Pin Assignments

5.6. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 6).

5.7. *RTL8752CGF Pin Assignments*

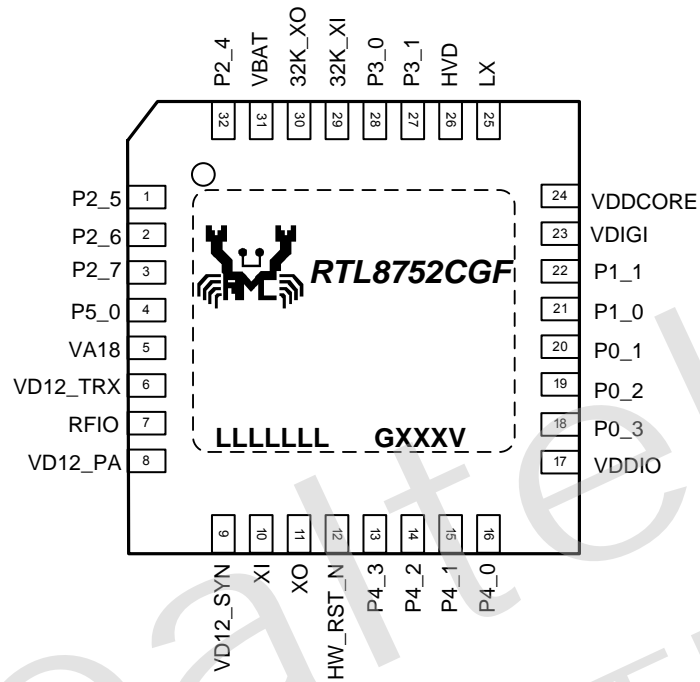


Figure 7. RTL8752CGF Pin Assignments

5.8. *Package Identification*

Green package is indicated by the 'G' in GXXXV (Figure 7).

6. Pin Descriptions

The following signal type codes are used in the tables:

I: Input

O: Output

P: Power

A: Analog

6.1. RF Interface

Table 1. RF Interface

Symbol	Type	Description			
		CJ	CJF	CRF/ CGF	
RFIO	A	9	9	9	BT RX /BT TX interface

6.2. XTAL and System Interface

Table 2. XTAL and System Interface

Symbol	Type	Description			
		CJ	CJF	CRF	
32K_XI	A/IO	38	37	29	32k crystal input or external 32k clock input (optional) Pin share as GPIO when external 32k is not used.
32K_XO	A/IO	39	38	30	32k crystal output (optional) Pin share as GPIO when external 32k is not used.
XI	A	12	12	10	40MHz crystal input
XO	A	13	13	11	40MHz crystal output or external 40MHz clock input
HW_RST_N	I	14	14	12	Hardware reset pin; low active

6.3. SPIC Interface (for External Flash)

Table 3. SPIC Interface (for External Flash)

Symbol	Type	Description			
		CJ	CJF	CRF	
SCLK	O	21	-	-	Clock output for flash
SO/SIO1	IO	24	-	-	Serial data output for one bit mode flash interface Serial data input/output for quad bit mode flash interface
CS#	O	23	-	-	Chip selection for flash
SI/SIO0	IO	22	-	-	Serial data input for one bit mode flash interface Serial data input/output for quad bit mode flash interface

6.4. General Purpose IOs

Table 4. General Purpose IOs

Symbol	Type	Description			
		CJ	CJF	CRF/ CGF	
P0_0	IO	-	26	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P0_1	IO	-	25	20	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P0_2	IO	-	24	19	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P0_3	IO	-	23	18	LOG_UART TX. Power on trap: Pull-up for normal operation Pull-down to bypass executing program code in flash (PAD internal pull-up by default).
P0_4	IO	-	22	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P0_5	IO	-	20	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P0_6	IO	-	19	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P1_0	IO	27	27	21	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. SWDIO (default).
P1_1	IO	28	28	22	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. SWDCLK (default).
P1_2	IO	19	-	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.

Symbol	Type	Description			
P1_3	IO	20	-	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. SIO3 (Quad-bit mode flash interface).
P1_4	IO	25	-	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. SIO2 (Quad-bit mode flash interface).
P2_2	IO	40	40	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. AUXADC input 2.
P2_3	IO	1	1	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. AUXADC input 3.
P2_4	IO	2	2	32	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. AUXADC input 4.
P2_5	IO	3	3	1	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. AUXADC input 5.
P2_6	IO	4	4	2	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. AUXADC input 6. Analog MIC input_N
P2_7	IO	5	5	3	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. AUXADC input 7. Analog MIC input_P
P3_0	IO	37	36	28	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. HCI_UART_TX (default).

Symbol	Type	Description			
P3_1	IO	36	35	27	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. HCI_UART_RX (default).
P3_2	IO	35	34	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P3_3	IO	34	33	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P3_4	IO	33	-	-	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P4_0	IO	18	18	16	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P4_1	IO	17	17	15	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P4_2	IO	16	16	14	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P4_3	IO	15	15	13	General purpose IO; refer to Table 9, Pin Multiplexer, page 20. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.

6.5. Power Pins

Table 5. Power Pins

Symbol	Type	Description			
		CJ	CJF	CRF/ CGF	
VA18	P	7	7	5	ADC reference voltage (decouple)
VD12_PA	P	10	10	8	Supply 1.2V power for PA
VD12_TRX	P	8	8	6	Supply 1.2V power for RF transceiver
VD12_SYN	P	11	11	9	Supply 1.2V power for synthesizer
VDDIO	P	-	21	17	Supply 1.8V~3.3V power for digital IO PADs
VDDCORE	P	30	30	24	Supply 1.2V power to LDO for digital core
VDIGI	P	29	29	23	1.1V digital power decouple
HVD	P	-	32	26	Supply 1.8V~3.3V power for Switching regulator input
LX	P	31	31	25	Switching regulator output
VBAT	P	32	39	31	Battery voltage input
MICBIAS/P5_0	P	6	6	4	Microphone bias (not available in RTL8752CGF) Pin share as GPIO when microphone bias is not used.

7. Bluetooth Radio

7.1. RF Transceiver

The RTL8752C includes an embedded GFSK RF transceiver with ultra-low power consumption and full compliance with the Bluetooth low energy wireless system. The block diagram is shown in Figure 8.

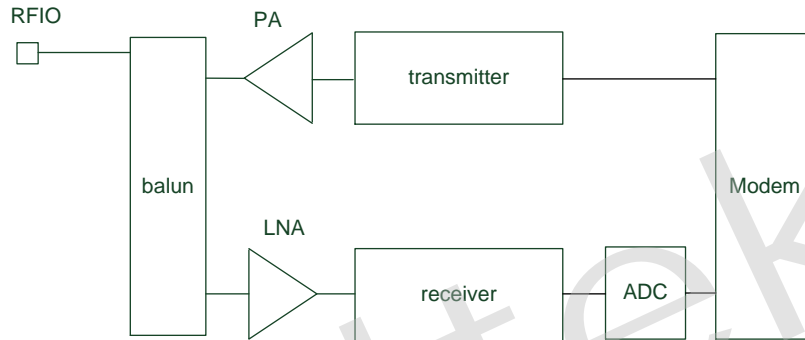


Figure 8. RF Transceiver Block Diagram

7.2. Modem

In the transmit path, the modem combines with the RF transmitter to generate a GFSK signal. In the receiver path, the modem receives a baseband GFSK signal from an analog to digital converter (ADC), and decodes the bit data via channel filtering, synchronizing, and demodulating.

An RF automatic calibration scheme is implemented in the modem to compensate for transistor characteristic variations in the CMOS process, and for ambient temperature differences.

7.3. Transmitter

The transmitter convert baseband signals to 2.4GHz unlicensed Industrial, Scientific and Medical (ISM) band GFSK modulated signals. The up-converted GFSK signal is amplified by the integrated power amplifier.

7.4. Front-End

To minimize external BOM requirements, the RTL8752C is single-ended RF mode and TX/RX path sharing the same RFIO pin with an integrated balun. For antenna matching and harmonic signal reduction, a PI matching network is required in the RF path.

8. Clock Management

For optimal power consumption and performance, the RTL8752C offers high and low frequency clocks. The high frequency clock is generated by an external 40MHz crystal oscillator (XTAL). The low frequency clock is generated by a 32.768kHz/32kHz XTAL.

In normal mode the high frequency clock is kept running to provide clock to the CPU, Bluetooth core, and the peripheral block. In low power mode the high frequency clock is turned off for power saving. The 32.768kHz/32kHz kHz low frequency clock remains on to provide clock to the RTC (Real Time Counter), BT core, and PMU.

8.1. 40MHz XTAL Oscillator

The RTL8752C has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the help of the internal built-in capacitor, the clock offset could be fine-tuned in the mass production process. The maximum internal cap is 20pF typically, and it is suggested to follow Realtek crystal design specification and QVL, the external capacitor, C_1 and C_2 , could be replaced by an internal capacitor, reducing the BOM cost, minimizing the PCB dimensions, and adding flexibility for clock fine tuning.

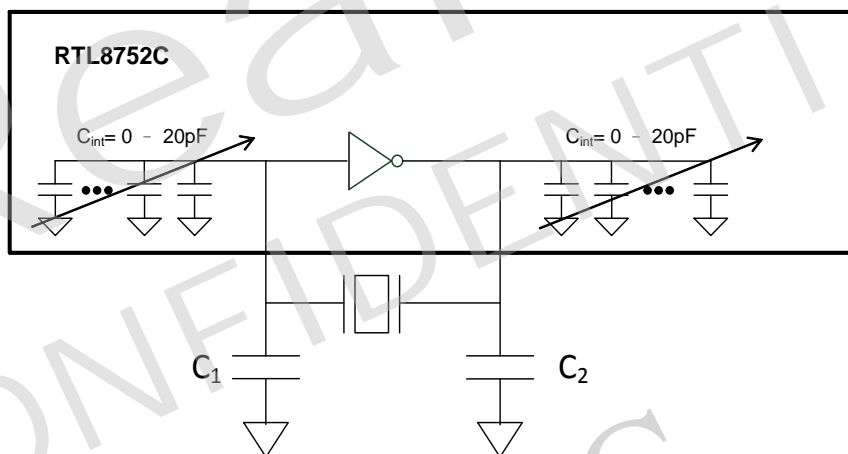


Figure 9. 40MHz Crystal Oscillation Schematic

Example:

For a crystal with spec $C_L=9\text{pF}$

$C_L = [(C_1 \times C_2) / (C_1 + C_2)] + (C_{\text{int}} / 2) + C_{\text{parasitic}}$, the parasitic capacitor $C_{\text{parasitic}}$ could be observed on the PCB trace and IC SMT soldering pad....etc.

With the rule of thumb, ' $C_1 + C_{\text{int}}$ ' is typical to be 12~15pF, hence the external capacitor C_1 and C_2 is possible to be replaced by the internal capacitor C_{int} , which could be 20pF at the maximum setting to over the need of external capacitors.

Table 6. 40MHz XTAL Specification

Parameter	Minimum	Typical	Maximum
Frequency (MHz)	-	40	-
Frequency tolerance (ppm)	-	-	±10
Frequency stability (ppm)	-	-	±10
Load capacitance (pF)	7	9	-
Maximum Drive Level (μW)	300	-	-
Equivalent Series Resistance (Ohm)	-	-	50Ω@7pF 40Ω@9pF
Insulation Resistance (MOhm)	500	-	-

8.2. 32kHz/32.768kHz XTAL Oscillator

The RTL8752C uses a 32kHz/32.768kHz XTAL oscillator as a sleep clock in low power mode. The block diagram of the XTAL Oscillator is shown in Figure 10. The 32kHz/32.768kHz XTAL specification is shown in Table 7, page 18.

There is a fixed 7pF capacitor (Cx) and a trimming capacitor (Cxi/Cxo) with a value from 0pF to 12.8pF in the RTL8752C. The embedded Cx, C1 and C2 are not required when a Crystal Load capacitor (CL) of 7pF is selected. The calculated value of Cxi, Cxo, C1, and C2 is shown in the following equation:

$$CL = \frac{(C1 + Cx + Cxi)(C2 + Cx + Cxo)}{(C1 + 2Cx + Cxi + C2 + Cxo)} + C_{stray}$$

If an external 32k crystal is not used, 32k_XI and 32k_XO pins can be configured as GPIO pins.

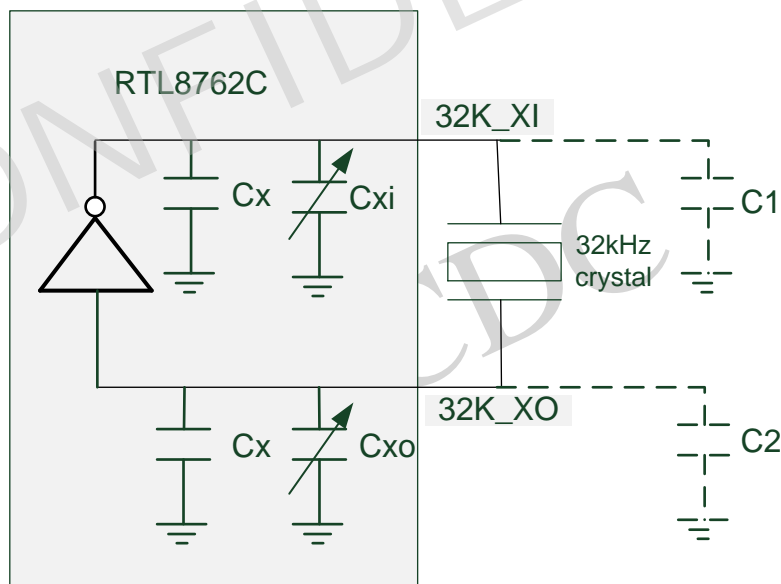

Figure 10. 32kHz Crystal Oscillator Schematic

Table 7. 32kHz XTAL Specification

Parameter	Minimum	Typical	Maximum
Frequency (kHz)	-	32.768 32	-
Frequency tolerance (ppm)	-	-	±20
Load capacitance (pF)	-	7	-
Maximum Drive Level (μW)	0.5	-	-
Equivalent Series Resistance (KOhm)	-	-	90
Insulation Resistance (MOhm)	500	-	-

8.3. Internal 32kHz RC Oscillator

The RTL8752C has a built-in internal 32K RCOSC used as a low speed clock source. With run-time self-calibration algorithm and limited user environment, temperature variation less than 1°C per second, the BLE link could be maintained via the internal 32K RC Oscillator.

9. Power Management Unit (PMU)

The RTL8752C is supplied with 1.8V to 3.3V by a single power source. For more flexibility of peripheral usage, IO voltage (VDDIO) can be different from VBAT in RTL8752CJF/CRF (but VDDIO should be less than or equal to VBAT). There is a high-efficiency BUCK regulator to provide power to the digital core circuit and radio circuit.

The RTL8752C defines three PMU power states for various conditions.

Active Mode: All clock and power is turned on. All functions operate in this mode.

Deep LPS Mode: High-speed clock and core domain power is turned off. The CPU stops running. Data can be retained in retention SRAM.

Power Down Mode: Except in an ‘always-on’ power domain, all clock sources and power are turned off. Power down mode can only be woken by GPIO pins.

10. Peripheral Interface Descriptions

The RTL8752C series peripheral descriptions are shown in the table below.

Table 8. Peripheral Interface Descriptions

Physical Address	IP Function
0x4000_0000 - 0x4000_0FFF	SYS Control
0x4000_1000 - 0x4000_17FF	GPIO
0x4000_2000 - 0x4000_2FFF	Timer
0x4000_3000 - 0x4000_37FF	IR RC
0x4000_4000 - 0x4000_47FF	Quad Decoder/2-Wire SPI
0x4000_5000 - 0x4000_57FF	Key Scan
0x4001_0000 - 0x4001_0FFF	AUXADC
0x4001_1000 - 0x4001_11FF	UART_1
0x4001_2000 - 0x4001_23FF	UART_0
0x4001_3000 - 0x4001_33FF	SPI_0
0x4001_3400 - 0x4001_37FF	SPI_1
0x4001_4000 - 0x4001_4FFF	AES engine
0x4001_5000 - 0x4001_53FF	I2C_0
0x4001_5400 - 0x4001_57FF	I2C_1
0x4002_0000 - 0x4002_0FFF	Reserved
0x4002_1000 - 0x4002_1FFF	Reserved
0x4002_4000-0x4002_43FF	UART_2
0x4002_4800-0x4002_4BFF	Reserved

10.1. Pin Multiplexer

All GPIO pins in the RTL8752C are configurable via the built-in pin multiplexer (PINMUX). Table 9 shows all GPIO pin configurations. Figure 11, page 21 shows the PINMUX and GPIO PADs control path. In the RTL8752C, all pins have an internal pull-up and pull-down resistor for controlling GPIO_PU and GPIO_PD.

Table 9. Pin Multiplexer (PINMUX)

0	IDEL	25	qdec_phase_a_z	50	SPI0_CLK (master only)	75	KEY_COL_17	100	Reserved	125	Reserved
1	HCI_UART_TX	26	qdec_phase_b_z	51	SPI0_MO (master only)	76	KEY_COL_18	101	Reserved	126	Reserved
2	HCI_UART_RX	27	UART2_TX	52	SPI0_MI (master only)	77	KEY_COL_19	102	PDM (clk)	127	Reserved
3	HCI_UART_CTS	28	UART2_RX	53	SPI2W_DATA (master only)	78	KEY_ROW_0	103	PDM (data)		
4	HCI_UART_RTS	29	UART1_TX	54	SPI2W_CLK (master only)	79	KEY_ROW_1	104	UART2_CTS		
5	I2C0_CLK	30	UART1_RX	55	SPI2W_CS (master only)	80	KEY_ROW_2	105	UART2_RTS		
6	I2C0_DAT	31	UART1_CTS	56	SWD_CLK	81	KEY_ROW_3	106	Reserved		
7	I2C1_CLK	32	UART1_RTS	57	SWD_DIO	82	KEY_ROW_4	107	Reserved		
8	I2C1_DAT	33	IRDA_TX	58	KEY_COL_0	83	KEY_ROW_5	108	Reserved		
9	PWM2_P	34	IRDA_RX	59	KEY_COL_1	84	KEY_ROW_6	109	Reserved		
10	PWM2_N	35	UART0_TX	60	KEY_COL_2	85	KEY_ROW_7	110	Reserved		
11	PWM3_P	36	UART0_RX	61	KEY_COL_3	86	KEY_ROW_8	111	Reserved		
12	PWM3_N	37	UART0_CTS	62	KEY_COL_4	87	KEY_ROW_9	112	Reserved		
13	PWM0	38	UART0_RTS	63	KEY_COL_5	88	KEY_ROW_10	113	Reserved		
14	PWM1	39	SPI1_SS_N_0 (master only)	64	KEY_COL_6	89	KEY_ROW_11	114	Reserved		
15	PWM2	40	SPI1_SS_N_1 (master only)	65	KEY_COL_7	90	DWGPIO	115	Reserved		
16	PWM3	41	SPI1_SS_N_2 (master only)	66	KEY_COL_8	91	Reserved	116	Reserved		
17	PWM4	42	SPI1_CLK (master only)	67	KEY_COL_9	92	Reserved	117	EN_EXPA		
18	PWM5	43	SPI1_MO (master only)	68	KEY_COL_10	93	Reserved	118	EN_EXLNA		
19	PWM6	44	SPI1_MI (master only)	69	KEY_COL_11	94	Reserved	119	ANT_SW0		
20	PWM7	45	SPI0_SS_N_0 (slave)	70	KEY_COL_12	95	Reserved	120	ANT_SW1		
21	qdec_phase_a_x	46	SPI0_CLK (slave)	71	KEY_COL_13	96	DMIC1_CLK	121	ANT_SW2		
22	qdec_phase_b_x	47	SPI0_SO (slave)	72	KEY_COL_14	97	DMIC1_DAT	122	ANT_SW3		
23	qdec_phase_a_y	48	SPI0_SI (slave)	73	KEY_COL_15	98	Reserved	123	Reserved		
24	qdec_phase_b_y	49	SPI0_SS_N_0 (master only)	74	KEY_COL_16	99	Reserved	124	Reserved		

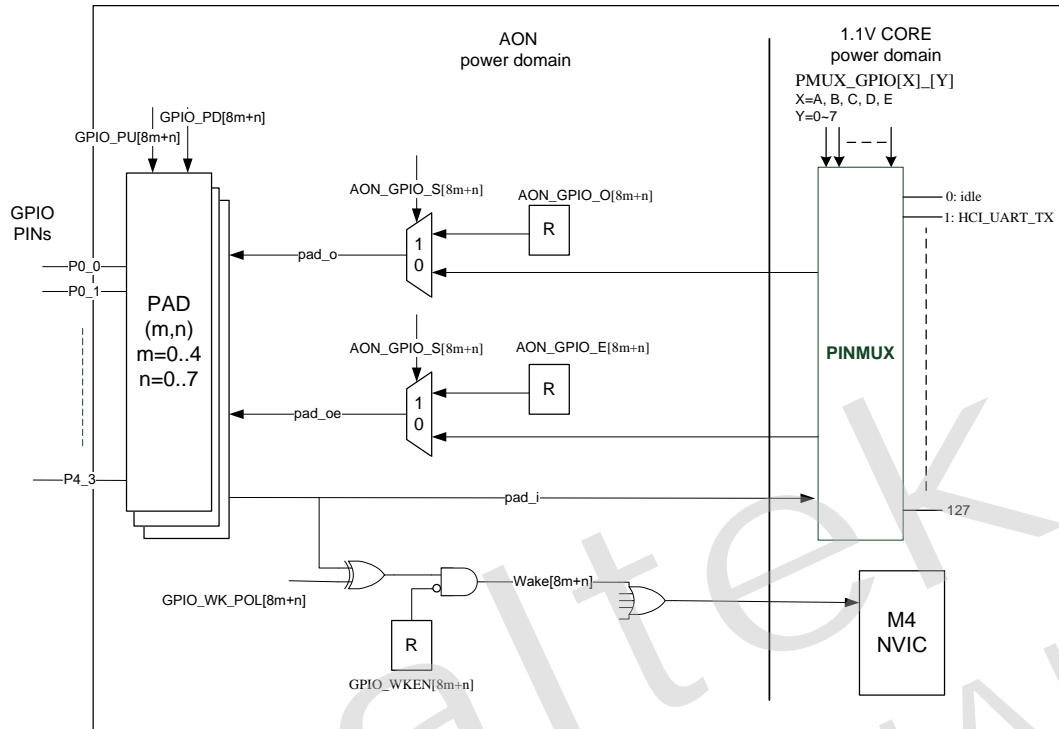


Figure 11. PINMUX and GPIO PADS Control Path

10.2. Real-Time Counter (RTC)

There are 24-bit counters with four individual comparators. The counter is clocked by an internal 32k RCOSC/external 32k XTAL with 12-bit pre-scalar. The comparators output can interrupt the CPU and wake up the chip from DLPS mode. The RTC block diagram is shown below.

Features:

- 12-bits pre-scale counter
- 24-bits read only RTC counter
- Internal 32k RCOSC/external 32k XTAL clock resource
- 4 independent comparators (with interrupt)
- 1 tick interrupt
- RTC counter overflow interrupt

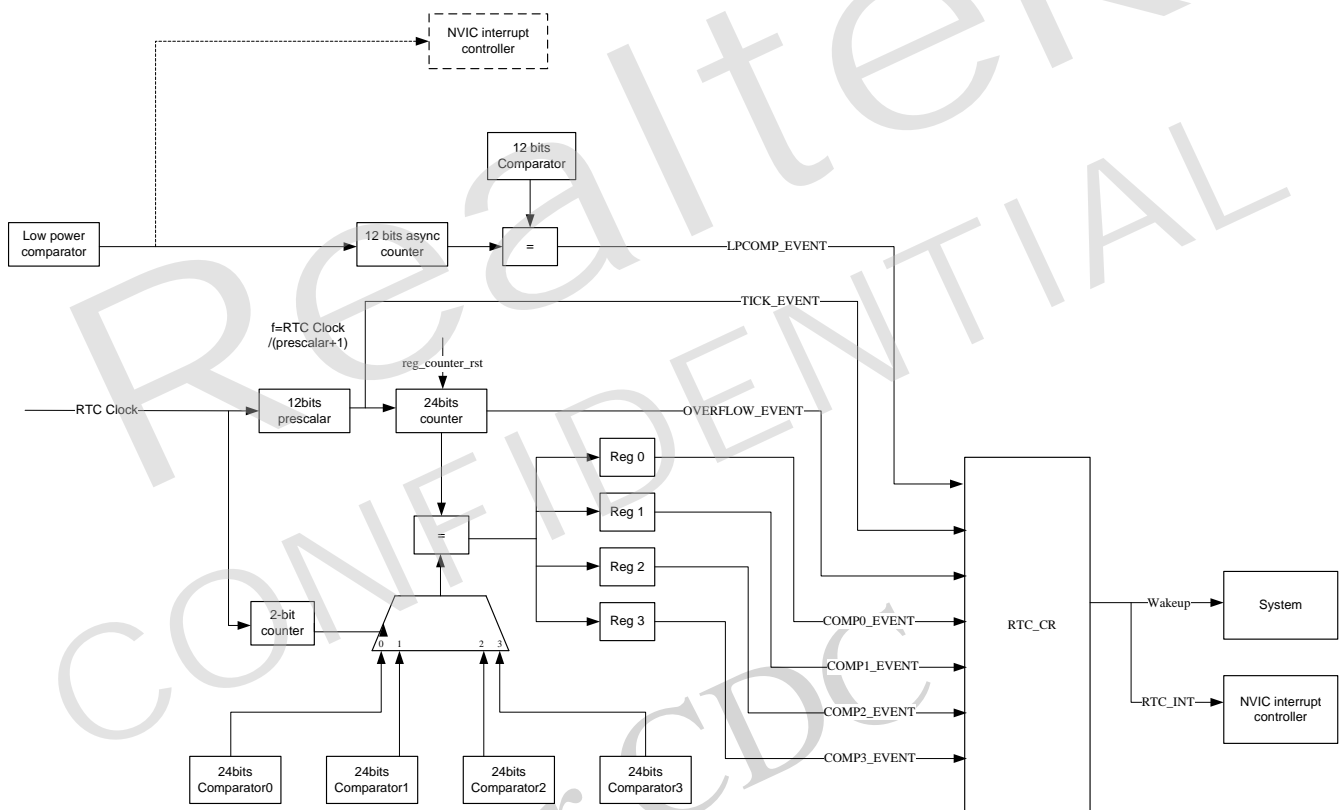


Figure 12. RTC Block Diagram

10.3. PWM /Hardware Timer (TIM)

The RTL8752C supports eight PWM/TIM modules.

The RTL8752C supports eight PWM/TIM modules.

Timer/PWM features:

- 8 independent Timers (2 Timers are dedicated for Internal use)
- Independent input clock divider 1/2 1/4, 1/8, 1/16, 1/40 (on all Timers)
- 3 mode (free run/ user define/PWM)
- 32bits counter
- Complementary PWM output & Dead zone (only Timer2, Timer3)
- PWM output state read back (<100kHz)

Table 10. Hardware Timer (Base Address: 0x4000_2000)

Address Range (Base +)	Function
0x00 to 0x10	Timer 0 Registers
0x14 to 0x24	Timer 1 Registers
0x28 to 0x38	Timer 2 Registers
0x3c to 0x4c	Timer 3 Registers
0x50 to 0x60	Timer 4 Registers
0x64 to 0x74	Timer 5 Registers
0x78 to 0x88	Timer 6 Registers
0x8c to 0x9c	Timer 7 Registers
0xb0 to 0xcc	TimerNLoadCount2 Registers

10.4. GPIO Control

The RTL8752C provides a highly flexible GPIO module for developers. There are 32 GPIOs assigned to IO PADs. The mapping table is shown in Table 11. GPIO function could be assigned to the IO PAD via the pin mux register.

Features:

- 32 GPIOs
- Input/output function
- 32 Independence interrupts
- 3 interrupt trigger conditions (level/edge/dual-edge)
- Hardware interrupt de-bounce

Table 11. GPIO Mapping Table

Pin Name	DWGPIO	Pin Name	DWGPIO	Pin Name	DWGPIO	Pin Name	DWGPIO	Pin Name	DWGPIO
P0_0	GPIO[0]	P1_0	GPIO[8]	P2_0	GPIO[16]	P3_0	GPIO[24]	MICBIAS /P5_0	GPIO[25]
P0_1	GPIO[1]	P1_1	GPIO[9]	P2_1	GPIO[17]	P3_1	GPIO[25]	32k_XI	GPIO[26]
P0_2	GPIO[2]	P1_2	GPIO[10]	P2_2	GPIO[18]	P3_2	GPIO[26]	32k_XO	GPIO[27]
P0_3	GPIO[3]	P1_3	GPIO[11]	P2_3	GPIO[19]	P3_3	GPIO[27]	P4_0	GPIO[28]
P0_4	GPIO[4]	P1_4	GPIO[12]	P2_4	GPIO[20]	P3_4	GPIO[28]	P4_1	GPIO[29]
P0_5	GPIO[5]	P1_5	GPIO[13]	P2_5	GPIO[21]	P3_5	GPIO[29]	P4_2	GPIO[30]
P0_6	GPIO[6]	P1_6	GPIO[14]	P2_6	GPIO[22]	P3_6	GPIO[30]	P4_3	GPIO[31]
P0_7	GPIO[7]	P1_7	GPIO[15]	P2_7	GPIO[23]	-	-	-	-

10.5. Quadrature Decoder

A three axis (X, Y, and Z-axis) quadrature decoder is built into the RTL8752C, including a smart interrupt mechanism to reduce firmware loading. The RTL8752C embeds the input debounce circuitry with the programmable timer.

Features:

- 2 input quadrature decoder
- 3 independent axis (X,Y, Z)
- Hardware de-bounce timer
- Configurable sample rate
- 16bits-counter
- Underflow/overflow interrupt

10.6. Hardware Key Scan

The RTL8752C supports a Configurable 12 rows * 20 columns key matrix with key scan engine. Each IO PAD could be configured as any row or column pin of Key Scan to reduce complexity of PCB routing. Features:

- Configurable matrix; max matrix (12 rows * 20 columns)
- Configurable matrix scan clock
- Configurable de-bounce time
- Configurable scan interval
- Configurable all-key release detect time
- 26 depth Key FIFO
- Key filter (one key)

10.7. IR Controller

The IR module provides a flexible way of transmitting and receiving IR code used in remote controls. It could send IR waveforms within the IR carrier, and receive IR waveforms within the IR carrier.

IR Transmitter Feature

- Programmable IR carrier (10kHz~60kHz)
- Programmable IR carrier duty
- Programmable IR carrier cycle number
- Hardware output waveform control
- TX FIFO Depth: 32

IR Receiver Feature

- Programmable sample clock (max clock 40MHz)
- Ability to learn IR waveform directly (carrier frequency = < 60kHz)
- Automatic/manual trigger mode
- Hardware waveform sample (not interfered with by software tasks)
- RX FIFO Depth: 32

10.8. SPI

There are two individual SPI interfaces in the RTL8752C. SPI0 supports master and slave mode. SPI1 supports master mode only.

SPI0 Features

- Master & slave mode
- Supports Clock Mode 0~3 (CPOL, CPHA)
- 4 transmit mode: TX only, RX only, Full-duplex, EEPROM
- 2*n SPI CLK Divider (Max 10MHz)
- Supports 4-32bits SPI data frame (master)
- Supports 4-16bits SPI data frame (slave)
- 1 Hardware CS (master)
- 32bits FIFO; 36 depth (master)
- 16bits FIFO; 64 depth (slave)
- DMA transfer supported

SPI1 Features

- Master mode
- Support Clock Mode 0~3 (CPOL, CPHA)
- 4 transmit mode: TX only, RX only, Full-duplex, EEPROM
- 2*n SPI CLK Divider (Max 10MHz)
- Supports 4-32bits SPI data frame (master)
- 3 Hardware CS (master)
- 32bits FIFO; 36 depth (master)
- DMA transfer supported

10.9. I2C

There are two separate I2C interfaces in the RTL8752C. Each I2C interface is comprised of Serial Data Line (SDA) and Serial Clock Line (SCL). Both I2C interfaces can be configured to master or slave mode.

Features:

- Master/Slave mode
- Supports 7/10 bits I2C address
- Configurable I2C address (slave mode)
- Standard speed (0-100kHz), Fast speed(100kHz~400kHz)
- TX FIFO 8 bits * 24
- RX FIFO 8bits * 40
- DMA supported

10.10. UART

There are three hardware UARTs (UART0, UART1, UART2), UART2 dedicated for log output. The UARTs have the same hardware features.

The RTL8752C provides multiple UART baud-rate configured by register setting. The common baud-rate example is shown in Table 12 below. The UART clock error between two devices should be less than $\pm 2.5\%$.

- Supports 7/8 Data Format
- 1/2 bit Stop bit
- Configurable parity bit: odd/even
- Programmable baud rate (max. baud rate 4,000,000)
- Hardware flow control
- RX line idle state detect
- DMA supported

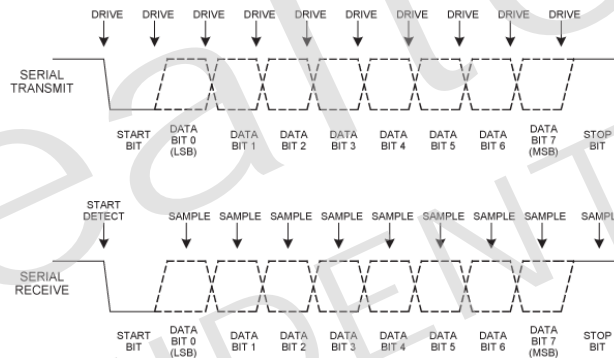


Figure 13. UART Waveform

Table 12. UART BaudRate

BaudRate (bps)	Error (%)	BaudRate (bps)	Error (%)
1200	-0.23	460800	0.17
9600	<0.01	500000	<0.01
14400	<0.01	921600	0.18
19200	<0.01	1000000	<0.01
28800	<0.01	1382400	0.17
38400	<0.01	1444400	-0.31
57600	<0.01	1500000	<0.01
76800	0.01	1843200	-0.35
115200	<0.01	2000000	0.02
128000	0.02	2764800	0.14
153600	-0.10	3000000	0.06
230400	0.03	4000000	0.03

10.11. Direct Memory Access Controller (DMA)

DMA features

- 6 DMA Channels
- Independent interrupts and control bit for every channel
- 4 transfer mode: Memory to memory, memory to peripheral, peripheral to memory, peripheral to peripheral
- Max block length 4095
- Multi-block supported (Channel 0 & 2)
- Scatter-gather supported (Channel 1 & 3)
- Safe abort/abnormal abort/suspend transfer
- Transferred items counter (single block)
- Hardware handshake interface for peripheral

10.12. AUXADC

The RTL8752C provides a built in (maximum 8 channels; the maximum number of ADC channels depends on the package type) 12bits, 400kbps AUXADC for external analog signal sensing and internal VBAT voltage monitoring. The functional block is shown in Figure 14.

- A 12bits, max 400ksps AUXADC with 8 channel sharing
- Flexible sampling schedule table for multi-channel sampling
- Divided mode: Support 0~VBAT input range with internal resistor divider
- Internal VBAT voltage sensing
- Supports single-ended mode and differential mode

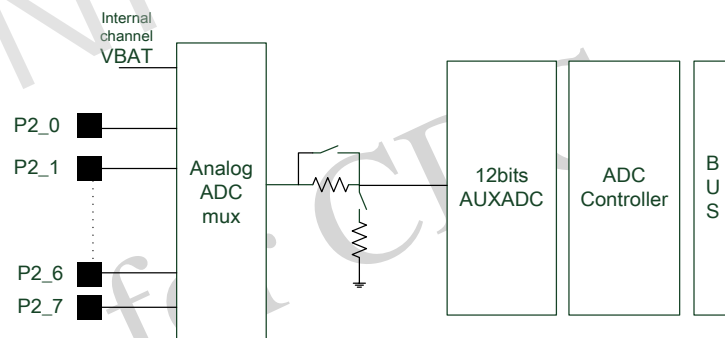


Figure 14. AUXADC Functional Block

10.13. Microphone Interface (not available in RTL8752CGF)

The analog microphone interface is constructed of a Programmable Gain Amplifier (PGA), Sigma-delta ADC, five-band equalizer, and decimation filter. The block diagram is shown in Figure 15.

The PGA helps amplify a weak signal from analog microphone. The sigma-delta ADC with decimation filter converts analog audio signals to digital audio signals with 16kHz; 16bits format.

The digital microphone interface pins, DMIC_CLK and DMIC_DATA, can be selected from the GPIO pins via the Mux pin.

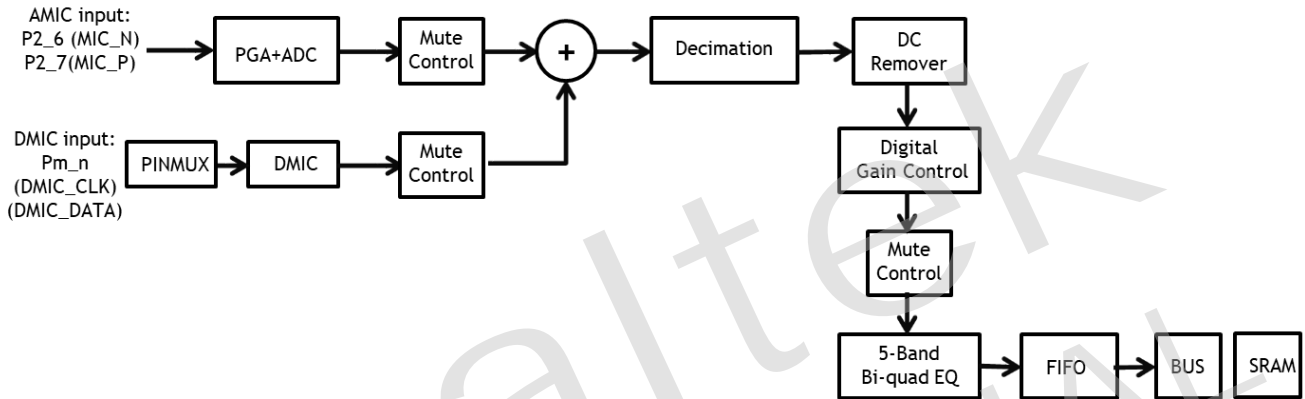


Figure 15. Microphone Interface

11. Electrical and Thermal Characteristics

11.1. Temperature Limit Ratings

Table 13. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	-40	85	°C

11.2. Power Supply DC Characteristics

Table 14. Power Supply DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VBAT	Single power source for whole chip	1.8	3	3.6	V
VDD_CORE VD12_PA VD12_RTX VD12_SYN	1.2V Core and RFAFE Supply Voltage	1.10	1.2	1.26	V
VDIGI	Digital core voltage	0.99	1.1	1.21	V
VDD_IO ^{Note}	Power for digital IO PADS	1.8	-	3.6	V
HVD	Power for switching regulator	1.8	-	3.6	V

Note: $VDD_IO \leq VBAT$

11.3. Switching Regulator Characteristics

Condition: VBAT=3V, VDDIO=3V, ambient temperature: 25°C

Table 15. Switching Regulator Characteristics

Parameter	Condition	Min	Typical	Max
Input voltage (V)	-	1.8	3	3.6
Output voltage (V)	-	-	1.2	-
Output current (mA)	Only for RTL8752C internal use	-	-	50
Recommended input capacitor (μF)	X5R	4.7	-	10
Recommended output capacitor (μF)	X5R	-	4.7	-
Recommended output inductor (μH)	1. Power inductor 2. +-20%	-	2.2	-

11.4. RTX LDO Characteristics

Condition: VBAT=3V, VDDIO=3V, ambient temperature: 25°C

Table 16. RTX LDO Characteristics

Parameter	Condition	Min	Typical	Max
Input voltage (V)	-	1.1	-	1.26
Output voltage (V)	-	-	1	-
Output voltage accuracy (%)	-	-5	-	5
Output current (mA)	Only for RTL8752C internal use	-	-	6
Quiescent current (μA)	-	-	40	-
PSRR	At 1kHz tone, vin= 1.2V	30	40	50

11.5. Synthesizer LDO Characteristics

Condition: VBAT=3V, VDDIO=3V, ambient temperature: 25°C

Table 17. Synthesizer LDO Characteristics

Parameter	Condition	Min	Typical	Max
Input voltage (V)	-	1.1	-	1.26
Output voltage (V)	-	-	1	-
Output voltage accuracy (%)	-	-5	-	5
Output current (mA)	Only for RTL8752C internal use	-	-	10
Quiescent current (μA)	-	-	40	-
PSRR	At 1kHz tone, vin= 1.2V	30	40	50

11.6. ESD Characteristics

Table 18. ESD Characteristics

Parameter	Condition	Minimum	Typical	Maximum
HBM	All pins, test method: JESD22	-	-	+/- 3.5 kV
MM	All pins, test method: JESD22	-	-	+/- 200 V
CDM	All pins, test method: JESD22	-	-	+/- 500 V

11.7. AUXADC Characteristics

Condition: VBAT=3V, VDDIO=3V, ambient temperature: 25°C

Table 19. AUXADC Characteristics

AUX Mode	Conditions	Min.	Typ.	Max.	Unit
Resolution	Bypass mode	-	12	-	BITS
	Divided mode (1/3.3)	-	12	-	BITS
Clock Source	From digital	-	-	400	kHz
DC Offset Error	After calibration (Bypass mode)	-	TBD	-	LSB
Gain Error	After calibration (Bypass mode)	-	TBD	-	LSB
DNL	Single-ended mode (Bypass mode)	-	+/-1.5	-	LSB
	Differential mode (Bypass mode)	-	+/-3	-	LSB
INL	Single-ended mode (Bypass mode)	-	+/-1	-	LSB
	Differential mode (Bypass mode)	-	+/-2	-	LSB
Input Voltage Range	External channel (ch0 ~ ch5) (Divided mode)	0	-	VBAT	V
	External channel (ch0 ~ ch5) (Bypass mode)	0	-	1	-
	Internal channel 0 (VBAT)	1.8	-	3.63	V
Input Impedance	Bypass mode	-	10	-	MOhm
	Resistor divider mode (1/4)	-	500	-	kOhm
Sampling Capacitance	Bypass mode	-	1.9	-	pF
	Resistor divider mode (1/4)	-	1.9	-	pF

11.8. Microphone Interface Characteristics

There are including PGA, sigma-delta ADC and MIC Bias characteristics.

Condition: VBAT=3V, VDDIO=3V, ambient temperature: 25°C

Table 20. Microphone Interface Characteristics

AUDIO Mode	Conditions	Min.	Typ.	Max.	Unit
Resolution	-	-	-	16	BITS
Input Sample Rate	-	8	16	16	kHz
Mode	-	-	Differential /Single-end	-	-
Signal to Noise Ratio (Single-ended mode)	Fin=1 kHz B/W=20~8 kHz A-weighted THD+N < 0.1 % 500mVrms input	-	TBD	-	dBA
Signal to Noise Ratio (differential mode)	Fin=1 kHz B/W=20~8 kHz A-weighted THD+N < 0.1 % 500mVrms input	-	90	-	dBA
Signal to Noise Ratio (Single-ended mode)	Fin=1 kHz B/W=20~8 kHz A-weighted THD+N < 0.5 % 5mVrms input 40 dB gain	-	TBD	-	dBA
Signal to Noise Ratio (differential mode)	Fin=1 kHz B/W=20~8 kHz A-weighted THD+N < 0.5 % 5mVrms input 40 dB gain	-	73	-	dBA
Digital Gain	-	-17.625		30	dB
Gain Step	-	-	0.375	-	dB
MIC Boost Gain	0/20/30/40 dB	0	-	40	dB
Input Full-Scale at Maximum Gain (Single-ended mode)	Gain = 40 dB	-	14.4	-	mVpp
Input Full-Scale at Maximum Gain (Differential)	Gain = 40 dB	-	28.8	-	mVpp
Input Full-Scale at Maximum Gain (Single-ended mode)	Gain = 0 dB	-	1.44	-	Vpp
Input Full-Scale at Minimum Gain (Differential)	Gain = 0 dB	-	2.88	-	Vpp
3dB Bandwidth		-	20	-	kHz
Microphone Mode Input Impedance	Input impedance	-	6	10	kOhm
	Input capacitance	-	-	20	pF

AUDIO Mode	Conditions	Min.	Typ.	Max.	Unit
THD+N@50mVrms Input (Single-ended mode)	AVDD=1.8V, Gain=20 dB	-	0.005	-	%
THD+N@100mVrms Input (Differential mode)	AVDD=1.8V, Gain=20 dB	-	TBD	-	%
THD+N@500mVrms Input (Single-ended mode)	AVDD=1.8V, Gain=0 dB	-	0.005	-	%
THD+N@1Vrms Input (Differential mode)	AVDD=1.8V, Gain=0 dB	-	TBD	-	%
MIC Bias	3-bits resolution	1.5	1.8	2.2	V

11.9. Radio Characteristics

Condition: VBAT=3V, VDDIO=3V, ambient temperature: 25°C

Table 21. General Radio Characteristics

Parameter	Condition	Minimum	Typical	Maximum
Frequency Range (MHz)	-	2402	-	2480

Table 22. RX Performance

Parameter	Condition	Minimum	Typical	Maximum
Sensitivity (dBm)	PER ≤ 30.8%	-97	-	-
Maximum Input Level (dBm)	PER ≤ 30.8%	-	-1	-
C/I	C/I _{co-channel} (dB)	21	-	-
	C/I _{+1MHz} (dB)	15	-	-
	C/I _{-1MHz} (dB)	15	-	-
	C/I _{+2MHz} (dB)	-17	-	-
	C/I _{-2MHz} (dB)	-15	-	-
	C/I _{+3MHz} (dB)	-27	-	-
	C/I _{image} (dB)	-9	-	-
	C/I _{image+1MHz} (dB)	-15	-	-
	C/I _{image-1MHz} (dB)	-15	-	-
Blocker Power (dBm)	30~2000MHz, Wanted signal level =-67dBm	-30	-	-
	2003~2399MHz, Wanted signal level =-67dBm	-35	-	-
	2484~2997MHz, Wanted signal level =-67dBm	-35	-	-
	3000MHz~12.75GHz, Wanted signal level =-67dBm	-30	-	-

Parameter	Condition	Minimum	Typical	Maximum
Max PER Report Integrity	Wanted signal: -30dBm	-	50%	-
Max Intermodulation level (dBm)	Wanted signal (f0): -64dBm Worst intermodulation level @2f1-f2=f0, f1-f2 =n MHz, n=3, 4, 5...	-50	-	-

Note: 1. Does not include spur channel

Note: 2. Depends on PCB design and registers setting

Table 23. TX Performance

Parameter	Condition	Minimum	Typical	Maximum
Maximum Output Power (dBm)	-	-	-	4
Adjacent Channel Power Ratio (dBm)	+2MHz	-	-	-20
	-2MHz	-	-	-20
	>=+3MHz	-	-	-30
	<=-3MHz	-	-	-30
Modulation Characteristics	$\Delta f_{1\text{avg}}$ (kHz)	-	250	-
	$\Delta f_{2\text{max}}$ (kHz)	185	-	-
	$\Delta f_{2\text{max}}$ Pass Rate (%)	-	100	-
	$\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$	-	0.88	-
Carrier Frequency Offset and Drift	Average Fn (kHz)	-	12.5	-
	Drift Rate (kHz/50μs)	-	10	-
	Avg Drift (kHz/50μs)	-	10	-
	Max Drift (kHz/50μs)	-	10	-
Output power of second harmonic(dBm)	-	-	-50(note)	-
Output power of third harmonic(dBm)	-	-	-50(note)	-

Note: Tested by EVB with RF PI network.

11.10. Digital IO Pin DC Characteristics

Table 24. Digital IO Pin DC Characteristics

Parameter	Condition	Min	Typical	Max
Input high voltage (V)	VDDIO=3.3V	2	3.3	3.6
Input low voltage (V)	VDDIO=3.3V	-	0	0.9
Output high voltage (V)	VDDIO=3.3V	2.97	-	3.3
Output low voltage (V)	VDDIO=3.3V	0	-	0.33
Input high voltage (V)	VDDIO=2.8V	1.8	2.8	3.1
Input low voltage (V)	VDDIO=2.8V	-	0	0.8
Output high voltage (V)	VDDIO=2.8V	2.5	-	
Output low voltage (V)	VDDIO=2.8V	0	-	0.28
Pull high and pull low resister (KOhm)	VDDIO=3.3V Strong pull/weak pull	-	10/100	-
	VDDIO=1.8V Strong pull/weak pull	-	20/200	-
	VDDIO=3.3V Strong pull/weak pull (P2_0~P2_7, MICBIAS)	-	5/50	-
	VDDIO=1.8V Strong pull/weak pull (P2_0~P2_7, MICBIAS)	-	2.5/25	-
Input high current (μA)	PAD configured as input mode	-	-	0.1
Input low current (μA)	PAD configured as input mode	-	-	0.1

11.11. Boot Sequence

The RTL8752C embeds a Power On Reset Circuit (POR), and power on sequence finite state machine to boot the system. Power on timing is shown in the figures below.

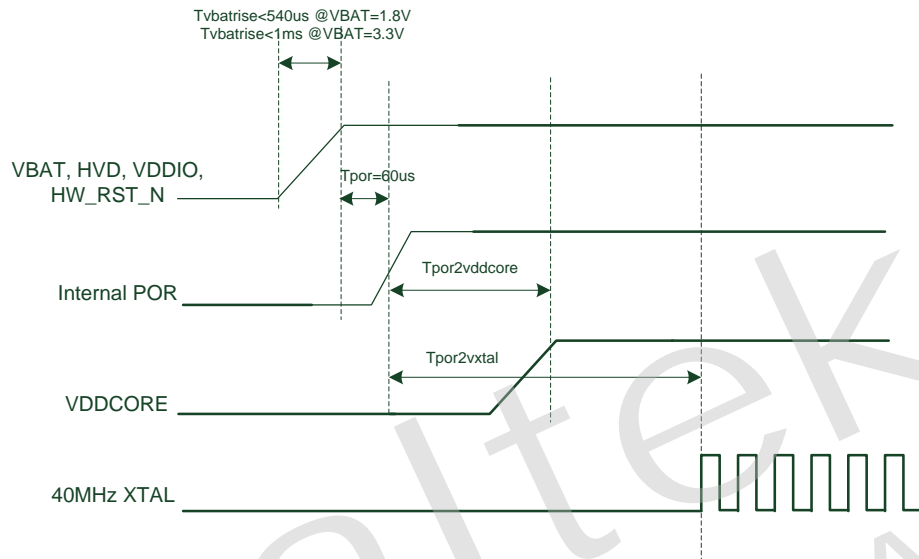


Figure 16. Boot Up By Internal Power On Reset Circuit

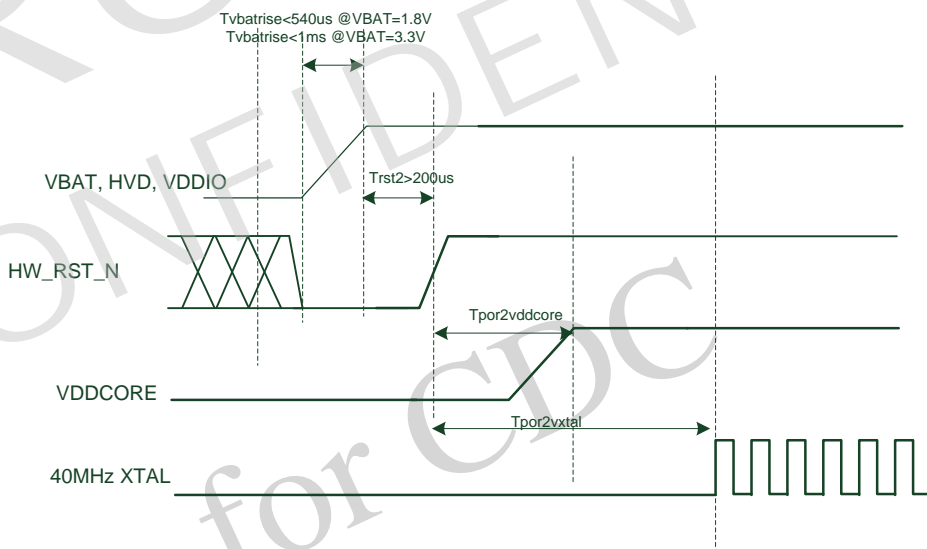


Figure 17. Boot Up By HW_RST_N Pin

11.12. UART Characteristics

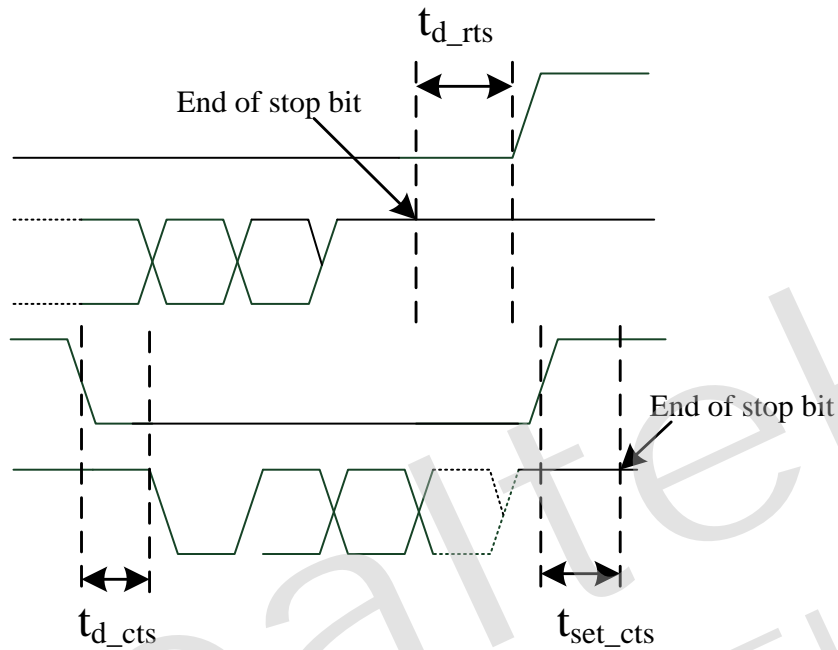


Figure 18. UART Characteristics

Table 25. UART Timing Characteristics

Parameter	Symbol	Min	Typical	Max
Timing between RX Stop bit and RTS go high when RX FIFO is full (symbol time)	t_{d_rts}	-	-	0.5
Timing between CTS go low and device send first bit (ns)	t_{d_cts}	-	-	25
Timing between CTS go high and TX send stop bit (ns)	t_{set_cts}	75	-	-

11.13. I2C Timing Characteristics

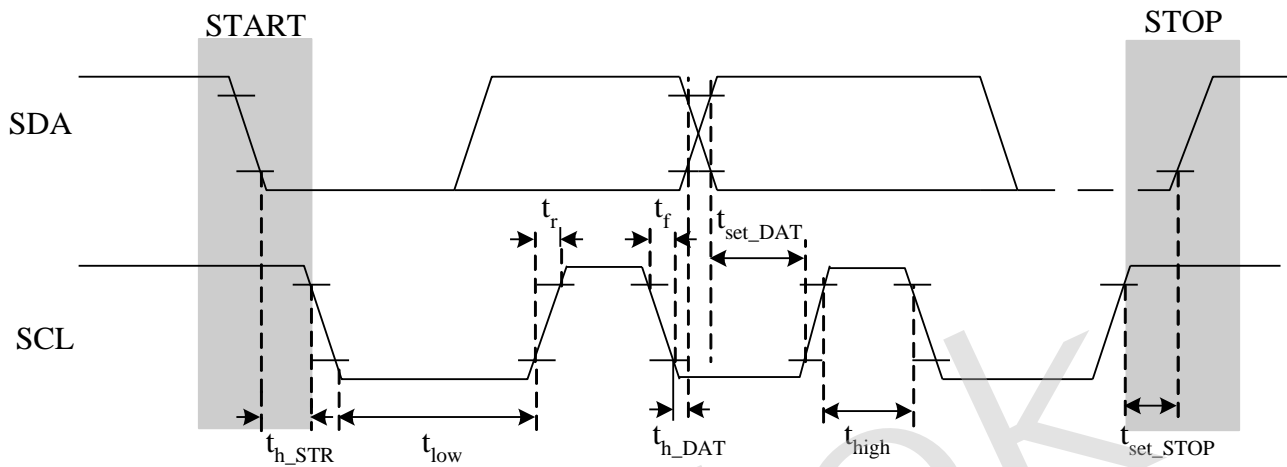


Figure 19. I2C Interface Timing Diagram

Table 26. I2C Timing Characteristics

Parameter	Symbol	Min	Typical	Max
SCL clock frequency (kHz)	-	-	-	400
High period of SCL (ns)	t_{high}	600	-	-
Low period of SCL (ns)	t_{low}	1300	-	-
Hold time of START (ns)	t_{h_STR}	600	-	-
Hold time of DATA (ns)	t_{h_DAT}	0	-	-
Setup time of STOP (ns)	t_{set_STOP}	600	-	-
Setup time of DATA (ns)	t_{set_DAT}	100	-	-
Rise time of SCL and SDA (ns) (with 4.7k ohm resistor pulled high)	t_r	See note	-	-
Fall time of SCA and SDA (ns)	t_f	See note	-	-

Note: Depends on the external bus pull up resistor.

11.14. Power Consumption

11.14.1. Low Power Mode

Condition: VBAT=3V, VDDIO=3V, ambient temperature: 25°C

Table 27. Low Power Mode

Power Mode	Always on Registers	32k RCOSC/XTAL	Retention SRAM	CPU	Wakeup Method	Current Consumption (typical)
Power down	ON	OFF	OFF	OFF	Wakeup by GPIO	450nA
Deep LPS	ON	ON	Retention	OFF	Wakeup by GPIO, timer	2.5μA (with 160K SRAM in retention state)

11.14.2. Active Mode

Condition: VBAT=3V, VDDIO=3V, ambient temperature: 25°C

Table 28. Active Mode

Power Mode	Current Consumption (Typical)
Active RX mode	7.3 mA
Active TX mode (TX power: 0dBm)	7.9 mA
Active TX mode (TX power: 4dBm)	9.6 mA

12. Mechanical Dimensions

12.1. RTL8752CJ/RTL8752CJF: Plastic Quad Flat No-Lead Package 40 Leads 5x5mm Outline

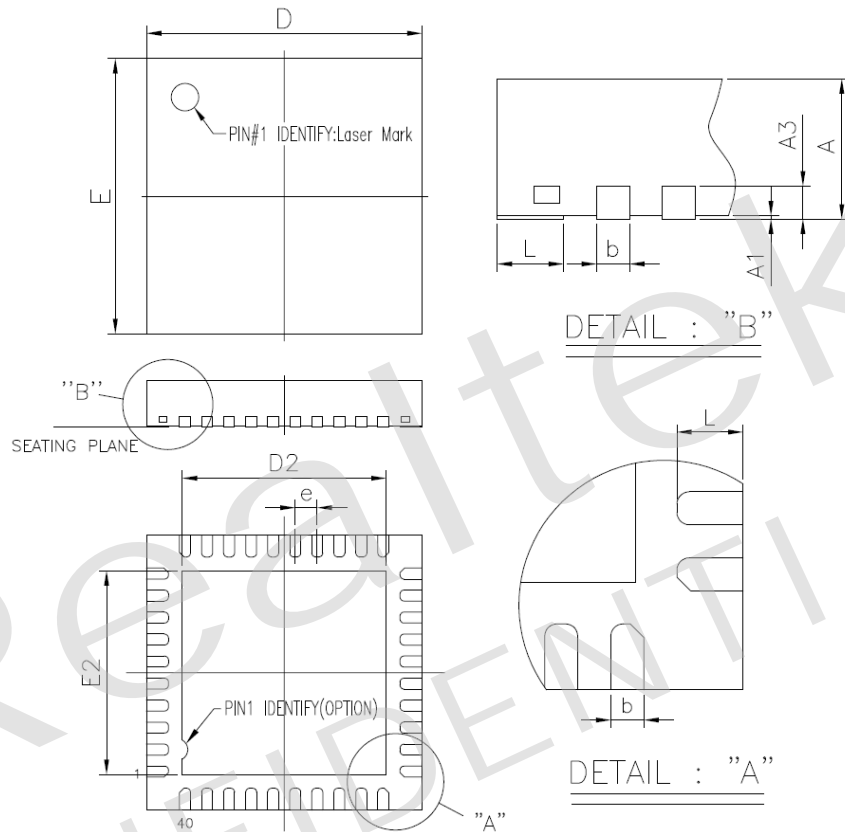


Figure 20. RTL8752CJ: Plastic Quad Flat No-Lead Package 40 Leads 5x5mm Outline

12.2. RTL8752CJ/RTL8752CJF Mechanical Dimensions Notes

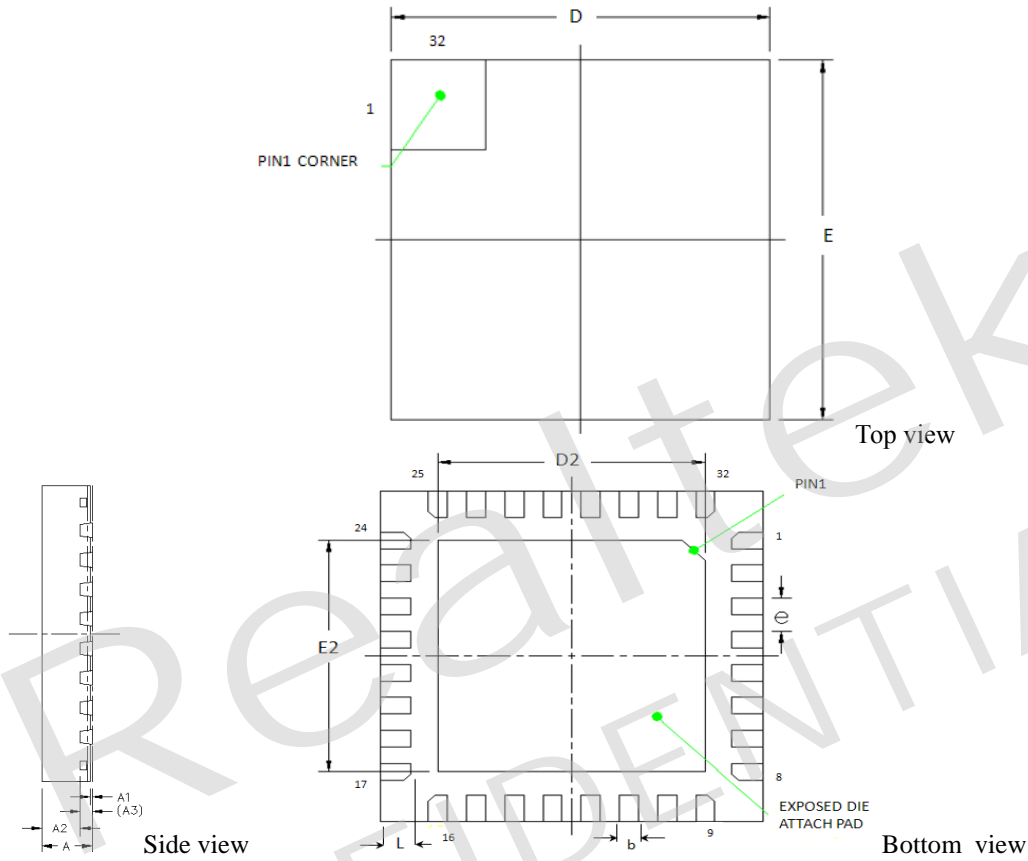
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.00 BSC			0.197 BSC		
D2/E2	3.45	3.60	3.75	0.136	0.142	0.148
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

CONTROLLING DIMENSION: MILLIMETER (mm).

REFERENCE DOCUMENT: JEDEC MO-220.

12.3. RTL8752CRF/RTL8752CGF: Plastic Quad Flat No-Lead Package 32 Leads 5x5mm² Outline



12.4. RTL8752CRF/RTL8752CGF Mechanical Dimensions

Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.000	0.035	0.050	0.000	0.001	0.002
A2	--	0.65	0.67	--	0.0256	0.0264
A3	0.200 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	5.00 BSC			0.20 BSC		
D2/E2	3.25	3.50	3.75	0.128	0.138	0.148
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes: CONTROLLING DIMENSION: MILLIMETER (mm).

REFERENCE DOCUMENT: JEDEC MO-220.

13. Reflow Profile

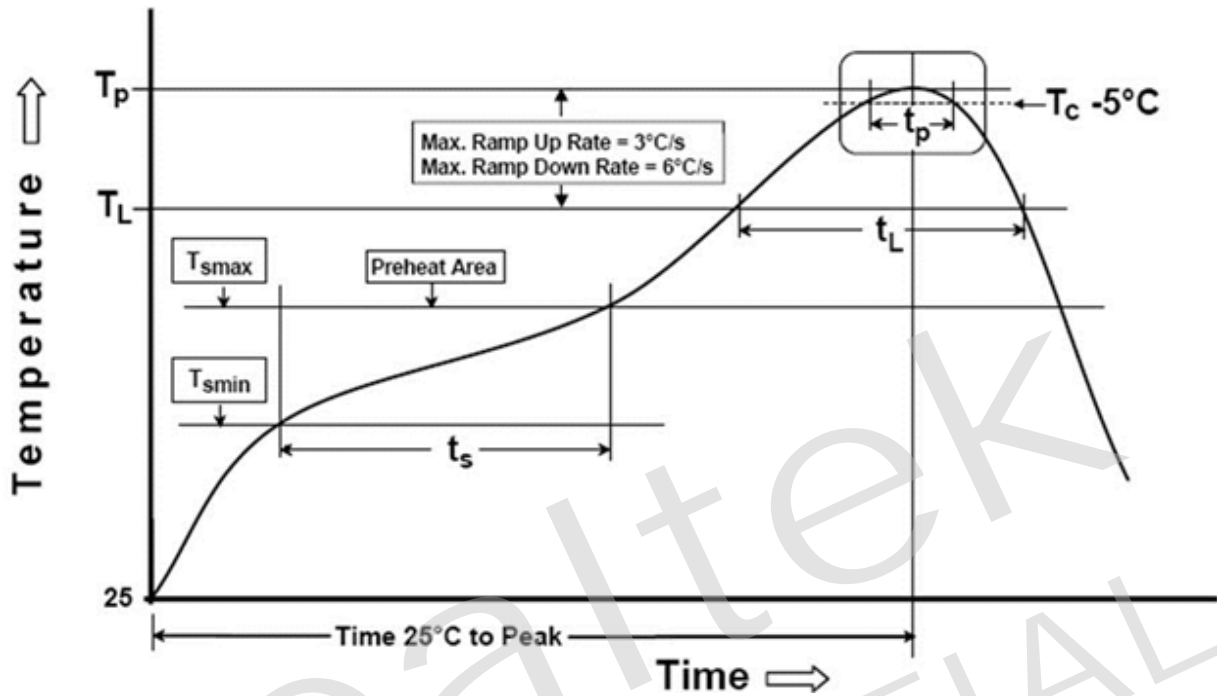


Table 29. Reflow Profile

Stage	Note	Pb-Free Assembly
Average ramp-up rate	T_L to T_p	3°C/ second max.
Preheat	Temperature min (T_{smin})	150°C
	Temperature max (T_{smax})	200°C
	Time (t_{smin} to t_{smax})	60 – 120 seconds
Time maintained above	Temperature(T_L)	217°C
	Time (t_L)	60 – 150 seconds
Peak package body temperature (T_p)		See following table. T_p must not exceed the specified classification temp in the following table.
Time(t_p) within 5°C of the specified classification temperature (T_c)		30 seconds
Ramp-down rate (T_p to T_L)		6°C / seconds max.
Time 25°C to peak temperature		8 minutes max.

Package Thickness	Volume < 350 mm ³	Volume 350 – 2000 mm ³	Volume > 2000 mm ³
< 1.6 mm	260 +0 /-5°C	260 +0/-5°C	260 +0 /-5°C
1.6 – 2.5 mm	260 +0 /-5°C	250 +0/-5°C	245 +0/-5°C
≥ 2.5 mm	250 +0 /-5°C	245 +0/-5°C	245 +0/-5°C

14. Ordering Information

Table 30. Ordering Information

Part Number	Package	Status
RTL8752CJ-CG	QFN-40, 5x5mm Outline; 'Green' Package	MP
RTL8752CJF-CG	QFN-40, 5x5mm Outline; 'Green' Package	MP
RTL8752CRF-CG	QFN-32, 5x5mm Outline; 'Green' Package	MP
RTL8752CGF-CG	QFN-32, 5x5mm Outline; 'Green' Package	MP

Note: See section 5 Pin Assignments, page 6 for package identification.

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